REMARKS

Claims 1-17 are pending in the application. In the Non-final Office Action mailed February 8, 2005, the Examiner indicated claims 8 and 15 comprised allowable subject matter. The Applicant thanks the Examiner for this indication of allowability. Claim 17 was rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. Accordingly, Applicant has canceled this claim. The remaining claims were rejected under 35 U.S.C. §103 as being obvious in view of Pawlowski (U.S. Patent No. 5,787,475).

The Applicant further thanks the Examiner for his time in conducting the telephone interview and the helpful comments made therein, and sincerely appreciates the Examiner's continued willingness to work with the Applicant on this application. The present amendment addresses the Examiner's concerns related to the need for additional structural elements and/or relationships between structural elements that would serve to distinguish the present invention over Pawlowski.

With regard to independent claims 1, 9 and 16, an element has been added to the claims related to the internal through connection of the integrated circuit configured to adaptively connect bits of the memory cells to the output terminals. This is supported in the originally filed specification by the last paragraph on p. 4 and carryover paragraph on p. 5. Support for the limitation that the data storage devices responds to a single data output request can be found on p. 2, lines 19-21. Applicant notes that the claimed structure *permits* the described memory access in response to a single request, but does not *require* that it always occurs in a single request. Therefore, the disclosure and claims are not at odds with the Specification

on p. 8, lines 12+ in which a special situation requiring two accesses are required. It is important to note that *Pawlowski* is distinguished in that it does not even <u>permit</u> the claimed data retrieval in a single access.

In paragraph 15 of the OA, p. 6, the Examiner discussed MPEP §2144.04 and *In re Larson* as well as *In re Tomoyuki Kohno* for the obviousness of integrating individual components into a one-piece construction, indicating that simply integrating the memory module and I/O module of Pawlowski into a single integrated circuit in order to increase processing speeds. In *Larson*, the court held that where the prior art taught several parts of a brake disc and clamp rigidly held together, simply using a one piece construction would be merely a matter of obvious engineering choice.

MPEP §2144.04(V)(B) also discusses the case *Schenck v. Nortron Corp.*, 713 F.2d 782 (Fed. Cir. 1983) in which the Federal Circuit found that an integration that eliminated a component presumed needed by the prior art was not obvious over the prior art.

The Applicant respectfully asserts that the present claims, as currently amended, go beyond a mere integration similar to that found in *Larson*, but rather are properly analyzed under the standard articulated in *Schenck*. The amendments to the claims go beyond the simple integration of the I/O and memory modules of Pawlowski into a single integrated circuit chip, because the amended claims now include the structure related to the through connection of the memory cells to the output terminals. This is substantively different than the memory and I/O

combination of Pawlowski in terms of the structure and appertaining function performed by the structure.

Since the goal of the invention pertains to a speed improvement, it is significant that this through connection be implemented on a single chip (and therefore, isolated from any sort of a shared system bus). The only element of Pawlowski that could arguably be likened to the claimed through connection is a system bus 16 (Pawlowski, Fig. 1) that is shared with the CPU 12 and presumably other hardware components.

Therefore, like the elimination of the resonance dampening mechanism in *Schenck*, the present invention eliminates the shared system bus over which Pawlowski's I/O module and main memory must operate (see Pawlowski at 2/3-7 discussing the need for retrieval using the system bus, and at 3/31-34 discussing the importance of not wasting system bus bandwidth; Pawlowski speaks in terms of *minimizing* a wasting of the system bus bandwidth (4/45-47), whereas the present invention *eliminates* a wasting of the system bus bandwidth). Furthermore, to the extent that Pawloski's system bus 16 is equated to the claimed through connection, Pawlowsky fails to teach an adaptive connection of bit for the memory to the output terminals of the data storage devices. Applicant's statements on p. 3, lines 11+ that "the data storage devices can also fundamentally be a matter of other arbitrary storage devices" was simply to indicate that the list of component types identified was not exhaustive, and not that any arbitrary aggregation of chip devices could be combined to create a "data storage device" according to the present invention. The

present amendment limiting the invention to a single integrated circuit unit is intended to clarify that distinction.

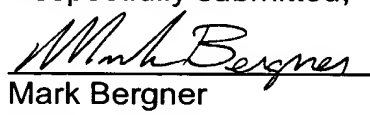
Applicant further notes that if the combination of the I/O module and main memory module of Pawlowski is being read on the data storage device of the present invention, then Pawlowski fails to teach that the amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request. The combination I/O module and main memory module of Pawlowski can be addressed by byte (see Pawlowski, Fig. 5, third column, and at 12/25, "As described above, the FBUS is byte addressable." Therefore, peripheral in Pawlowski can ask the combination I/O module and main memory module for a single byte at a specific memory location. This would correspond to memory that is addressable on individual byte boundaries and capable of returning a single byte in response to the request. However, the independent claims require that the selectable output start addresses be spaced such that (a) an amount of data that can be stored between neighboring output start addresses is smaller than (b) an amount of data output in response to the data output request. The teaching of Pawlowski is not that (a) is smaller than (b), as required by the claims, but that (a) is equal to (b), i.e., a single byte.

For this reason, the Applicant asserts that the amended claim language clearly distinguishes over the prior art, and respectfully requests that the Examiner withdraw the §103 rejection from the present application. Applicant welcomes any suggestions by the Examiner with regard to claim language.

CONCLUSION

Inasmuch as each of the rejections have been overcome by the amendments and arguments presented, and all of the examiner's suggestions and requirements have been satisfied, it is respectfully requested that the present application be reconsidered, the rejections be withdrawn and that this application be passed to issue.

Respectfully submitted,



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